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| EXAMINER | |
|---|---|
| NGUYEN, LONG T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/777,174 | KOCH ET AL. | |
| | Examiner | Art Unit | |
| | Long Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3,7-12,14,16-18 and 20-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7-11,20,21,23,27 and 28* is/are rejected.

7)☒ Claim(s) *12,14,16-18,22,25,26 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 1, 3, 7-12, 14, 16-18, and 20-29 are objected to because of the following informalities:

Claim 1, lines 13-15, "of the first transistor, the capacitor being connected across the gate electrode of one of said transistors" should be changed to --of one of said transistors, the capacitor being connected across the gate electrode said one of said transistors--.

Claims 3, 7-12 and 25-27 are objected to because they include the informalities of claim 1.

Claim 11, line 1-2, "wherein the inverter including another PFET and another NFET" should be changed to --wherein the field effect transistors of the inverter including another PFET and another NFET-- so that the claim is clear because claim 8 (which claim 11 depends on) already recited that the inverter having field effect transistors.

Claim 11, line 2, "the PFET" should be changed to --the another PFET--.

Also, in claim 11, line 6, "inverters" should be changed to --inverter-- to avoid lacks antecedent basis since there is only "the inverter" recited earlier (see line 1 of claim 11).

Claims 12, 25 and 16 are objected to because they include the informalities of claim 11.

Claim 12, line 7, "on.." should be changed to --on.--.

Claim 14, line 40, "switched on, each of the inverters including a PFET and an NFET" should be changed to --switched on, wherein the transistors of each of the inverters including a PFET and an NFET-- so that the claim is clear (because lines 30 and 35 of the claim already

recited that the first inverter comprises third and four transistors and the second inverter comprises fifth and sixth transistors).

Claims 16-18 and 22 are objected to because they include the informalities of claim 14.

Claim 20, line 8, "the transistor" should be changed to --the first transistor--.

Claim 20, line 31, "inverter the source" should be changed to --inverter, the source--.

Claim 21 and 23 are objected to because they include the informalities of claim 20.

Claim 24, lines 13-15, "of the first transistor, the capacitor being connected across the gate electrode of one of said transistors" should be changed to --of one of said transistors, the capacitor being connected across the gate electrode said one of said transistors--.

Claim 24, line 24, "said one transistor" should be changed to --said one of said transistors-- for consistency (see line 19 of the claim) .

Claim 24, line 27, "said one field effect transistor" should be changed to --said one of said transistors-- for consistency (see line 19 of the claim) .

Claim 24, line 28, "the inverter including another PFET and another NFET" should be changed to --wherein the field effect transistors of the inverter including another PFET and another NFET-- so that the claim is clear because line 25 already recited that the inverter having field effect transistors.

Claim 24, line 31, "PFETs" and "NFETs" should be changed to --PFET-- and --NFET--, respectively.

Claim 24, line 32-33, "of each of the inverters" should changed to --the inverter-- because the switching circuit comprises "an inverter" (see line 24-25, not a plural of inverters--.

Claim 24, line 40, --the-- should be inserted before "another PFET".

Claim 25, line 8, "on.." should be changed to --on.--.

Claim 28, line 22, "the other of the transistors" should be changed to --the second of the transistors-- to provide antecedent basis that is consistent with the later recitations (see line 26 of claim 28, and line 3 of claim 29).

Claim 29 is objected to because it includes the informality of claim 28.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 24, the recitation "insubstantial current flows through the resistor while another PFET is switched off" on lines 39-40 of the claim is indefinite because it is inconsistent with what already recited earlier. Note that, line 38-39 of the claim recited that substantial current flows through the resistor while the another NFET is switched on, so it would be contradicted to recited "insubstantial current flows through the resistor while another PFET is switched off" on lines 39-40 because: in Figure 1 of the instant application, the another NFET would be element 38 and the resistor would be element 40 to meet the recitation "substantial current flows through the resistor while the another NFET is switched on" so the another PFET must be element 36. Therefore, if the another PFET (36, Figure 1) is switched off then the another NFET 38 in Figure 1 must be switched on and thus substantial current still flows through

the resistor 40. Thus, the recitation "insubstantial current flows through the resistor while another PFET is switched off" on lines 39-40 of the claim is indefinite.

***Claim Rejections – 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 7-11, 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki et al. (USP 5,694,065) in view of Love (USP 5,068,553).

With respect to claims 1, 3 and 27 Figure 2 of the Hamasaki et al. reference discloses a circuit which includes a first terminal (IN); a driver (50, 60) having a first transistor (PFET 50) and a second transistor (NFEF 60) each having a source drain path; output terminal (OUT); first (ground supply) and second (5V supply) opposite power supply terminals; and pulse shaping circuitry (72, 74, Rn, Cn, 82, 84, Rp and Cp) for (a) causing the first and second source drain paths to be respectively (i) on and off while the voltage source has the first level (5V) and (ii) off and on while the voltage source (IN) has the second level (0V), and (b) preventing both source drain paths from being on simultaneously (lines 60 of Col. 5 to line 21 of Col. 6); wherein the pulse-shaping circuitry comprising a resistive element (resistor Rn) and a capacitor (Cn), the resistive element (Rn) being connected for supplying current to the capacitor (Cn) and the gate electrode of the first transistor (PFET 50), the capacitor (Cn) being connected a gate electrode of the first transistor (PFET 50) and the first power supply terminal (ground supply), the first power supply terminal (ground supply) being connected for supplying current to the source drain path

of the second transistor (NFET 60) while the second transistor (NFET 60) is on. Figure 2 of the Hamasaki et al. reference does not disclose that the first capacitor (Cn) comprising an n-channel field effect device (i.e., transistor having a conductivity type opposite to the conductivity type of the PFET first transistor 50). However, the Love reference discloses that a capacitor is easily formed by using an NMOS transistor that has its drain and its source connected together (see capacitor 26 in Figure 1, or capacitor 80 in Figure 3). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 2 of the Hamasaki reference to use specific capacitor-connected NMOS transistor (as taught by the by the Love reference) for broad capacitor elements in the circuit of Figure 2 of the Hamasaki reference (i.e., each of the capacitors Cn and Cp in Figure 2 is implemented by a capacitor-connected NMOS transistor) for the purpose of easily integrated the circuit. Thus, this modification/combination meets the limitations of claim 1 because the capacitor (Cn) being a FET device (n-channel FET as discussed) having a conductivity type opposite from the of the first of the transistors (i.e., PFET 50). Note that all the elements (resistor Rn, capacitor Cn, PFET 50 and NFET 60) are included in an integrated circuit chip (claim 3), and the voltage source (IN) has transitions in both directions between the first and second levels (see lines 60 of Col. 5 to line 21 of Col. 6, Hamasaki et al.).

With respect to claims 7-9, Figure 2 of Hamasaki et al. in the above combination shows the pulse shaping circuitry including the a switching circuit (72, 74) having an input terminal and an output terminal, the output terminal of the switching circuit being connected so current can flow via a DC path between (a) the first power supply terminal (ground) and (b) the capacitor and the gate electrode of the first transistor, wherein the DC path including the resistive element

Rn (i.e., when transistor 74 is ON, then current flows through a DC path from ground through the source-drain of transistor 74 and through the resistor Rn to the gate of PFET 50 and capacitor Cn); wherein the pulse-shaping circuitry comprising an inverter (72, 74) having FETs, wherein all the FETs of the inverter are included in an integrated circuit chip including a resistor (Rn) comprising the resistive element (Rn).

For claims 10 and 11, for broadest reasonable interpretation, the combination of elements 72, 74 and Rn forms an inverter, and thus the output of inverter is signal D01, so it meets the limitation the resistive element included in the inverter, wherein inverter also comprises another PFET (72) and another NFET (74). Figure 2 of the Hamasaki et al. reference does not disclose that the first capacitor (Cn) comprising a field effect device having a conductivity type opposite to the conductivity type of the first transistor (PFET 50).

Insofar as understood in claim 24, this claim is rejected for the similar reasons as discussed in claims 1, 3 and 7-11 above. Note that substantial current flows through the resistor (Rn) when the another NFET (74) is switched ON and while the another PFET (72) is switched off (as discussed above under 35 U.S.C 112, 2$^{nd}$ paragraph that while the another PFET is switched off then substantial current still flows through the resistor).

With respect to claim 28, Figure 2 of the Hamasaki et al. reference discloses a circuit which includes a first terminal (IN); a driver (50, 60) having a first transistor (PFET 50) and a second transistor (NFEF 60); output terminal (OUT); pulse shaping circuitry (72, 74, Rn, Cn, 82, 84, Rp and Cp) comprising a resistive element (resistor Rn) and a capacitor (Cn); first (5V power supply) and second (ground supply) opposite power supply terminals for respectively providing first and second DV voltages (5V and 0V). Figure 2 of the Hamasaki et al. reference does not

disclose that the first capacitor (Cn) comprising an n-channel field effect device (i.e., transistor having a conductivity type opposite to the conductivity type of the PFET first transistor 50). However, the Love reference discloses that a capacitor is easily formed by using an NMOS transistor that has its drain and its source connected together (see capacitor 26 in Figure 1, or capacitor 80 in Figure 3). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 2 of the Hamasaki reference to use specific capacitor-connected NMOS transistor (as taught by the by the Love reference) for broad capacitor elements in the circuit of Figure 2 of the Hamasaki reference (i.e., each of the capacitors Cn and Cp in Figure 2 is implemented by a capacitor-connected NMOS transistor) for the purpose of easily integrated the circuit. Thus, this modification/combination meets the limitations of claim 28 because the capacitor (Cn) being a FET device (n-channel FET as discussed) having a conductivity type opposite from the of the first of the transistors (i.e., PFET 50) and including first and second electrodes connected between the gate electrode of the first of the transistors and the power supply terminal (ground) for supplying current directly to the source drain path of the second of the transistors (i.e., NFET 60).

6. Claims 20, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chehadi (USP 6,437,609) in view of Wanlass (USP 3,356,858).

Note that Figure 8 discloses a circuit, which includes: a first terminal (E) for receiving a voltage source (E); a driver (inverter I); an output terminal (S); and pulse-shaping circuitry (Tx, Ty, R, C); first and second opposite power supply terminals (ground and Vcc terminals), wherein the pulse-shaping circuitry including: (a) a switching circuit (Tx, Ty, R) including a resistive element (R) and an output terminal (connected to input of inverter I), wherein the switching

circuit including an inverter (Tx, Ty, R) comprising second and third transistors (Tx and Ty) and the resistive element (R); and (b) a capacitor (C). The Chehadi reference does not discloses that the inverter I comprise a PFET and an NFET. However, the Wanlass reference discloses in Figure 5 that an inverter is easily formed by using a PFET connected with an NFET transistor that provides advantage such as low power consumption. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 8 of Chehadi by using the inverter having a PFET and an NFET as taught in Figure 5 of Wanlass for the inverter I (Figure 8, Chehadi) for the purpose of reduce power consumption. Thus, this modification/combination meets all the limitations of claims 20, 21 and 23 as specifically discussed below.

With respect to claims 20, 21 and 23, the modification of Figure 8 of Chehadi as discussed above discloses a circuit which includes a first terminal (E); a driver (PFET and NFET inside of inverter I) having a first transistor (PFET); output terminal (S); first (ground) and second (power Vcc) opposite power supply terminals; pulse shaping circuitry (Tx, Ty, R, C) comprising: a switching circuitry (Tx, Ty, R) including an output terminal (terminal directly connected to the input of inverter I) that is DC connected to the control electrode of the first transistor (PFET inside I), and a capacitor (C) connected between the control electrode of the first transistor (PFET inside I) and the first power supply terminal (ground), the switching circuitry (Tx, Ty, R) further including a resistive element (resistor R) and second and third transistors (Tx, Ty) that is formed an inverter (Tx, Ty, R), wherein the resistive element (R) is connected between the source-drain path of the third transistor (Ty) and the output terminal (terminal connected to the input of inverter I) of the inverter (Tx, Ty, R), wherein the source

drain path of the second transistor (Tx) being connected directly between the output terminal of the inverter and one of the power supply terminals (Vcc) that the voltage at the one power supply terminal (Vcc) is always applied directly to the output terminal of the inverter via the source drain path of the second transistor (Tx) while the source drain path of the second transistor (Tx) is switched on. Note that the resistor (R) is connected such that substantial current flows through the resistor while the third transistor (Ty) is switched on and insubstantial current flows through the resistor while the third transistor (Ty) is switched off and the second transistor (Tx) is switched on.

***Allowable Subject Matter***

7. Claims 14, 16-18, 22 presently would be allowed if amend to overcome the informalities set forth above.

8. Claims 12, 25, 26 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if amended to overcome the minor informalities set forth above.

***Response to Arguments***

9. Applicant's arguments filed on 6/22/06 have been fully considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER